PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Simon DELEONIBUS

Group Art Unit: 2826

Application No.: 10/591,863

Examiner: W. Kuo

Filed: September 6, 2006

Docket No.: 129344

For: FIELD EFFECT TRANSISTOR WITH SUITABLE SOURCE, DRAIN AND CHANNEL MATERIALS AND INTEGRATED CIRCUIT COMPRISING SAME

SUBMISSION OF TRANSLATION OF FOREIGN PRIORITY DOCUMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the Examiner's request made during the February 28, 2008 personal interview, attached is a translation of French Application No. 043066 filed on March 25, 2004, which is the foreign priority document for the above-identified application. Upon information and belief, the translation is an accurate English translation of the foreign priority document as filed.

Respectfully submitted,

William P. Berridge
Registration No. 30,024

John A. Radi
Registration No. 59,345

WPB:MIL/hms

Attachment:
Translation of FR 043066

Date: March 14, 2008

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

Field effect transistor with suitable source, drain and channel materials and integrated circuit comprising same

Background of the invention

The invention relates to a field effect transistor comprising a source, a drain and a channel, respectively formed by source, drain and channel materials.

State of the art

Field effect transistors achieved on a thin film conventionally comprise a source and a drain connected by a channel controlled by a gate electrode. The charge carriers are slowed down by diffusion when passing in the channel on the one hand, and between the source and the channel on the other hand, which limits the switching velocity of the transistor. Typically, to solve this problem, the source and drain zones are strongly doped, which requires a strong activation of the dopants in the source and drain materials. If these materials are semi-conductors, activation of the dopants is limited by the limited chemical solubility of the dopants in the materials.

Object of the invention

It is one object of the invention to remedy these shortcomings and, in particular, to produce transistors enabling faster operation.

According to the invention, this object is achieved by the fact that source, drain and channel materials are selected such that, for a NMOS transistor, the electronic affinity of the drain material is lower than the electronic affinity of the channel material and such that, for a PMOS transistor, the upper level

of the valence band of the drain material is higher than the upper level of the valence band of the channel material.

According to a first embodiment of the invention, the transistor being of the normally on type, the electronic affinity of the source material of a NMOS transistor is higher than the electronic affinity of the channel material of said NMOS transistor and the upper level of the valence band of the source material of a PMOS transistor is lower than the upper level of the valence band of the channel material of said PMOS transistor.

According to a second embodiment of the invention, the transistor being of the normally off type, the electronic affinity of the source material of a NMOS transistor is lower than the electronic affinity of the channel material of said NMOS transistor and the upper level of the valence band of the source material of a PMOS transistor is higher than the upper level of the valence band of the channel material of said PMOS transistor.

It is a further object of the invention to provide an integrated circuit comprising PMOS and NMOS type field effect transistors according to the invention.

Brief description of the drawings

Other advantages and features will become more clearly apparent from the following description of particular embodiments of the invention given as non-restrictive examples only and represented in the accompanying drawings, in which:

Figures 1 to 5 illustrate a particular embodiment of a method for producing a transistor according to the invention.

Description of particular embodiments

The transistors according to the invention each comprise a channel made of a predefined material, for example silicon (Si), germanium (Ge), diamond-like carbon (diamond-like C), gallium arsenide (GaAs) or indium antimonide (InSb).

According to the invention, the source and drain materials of NMOS transistors are selected according to their electronic affinities Xs and Xd, whereas for PMOS transistors, the source and drain materials are selected according to their upper levels Es and Ed of the valence band.

The drain material of a NMOS transistor is selected such that the electronic affinity Xd of the drain material is lower than the electronic affinity Xc of the channel material of said NMOS transistor (Xd<Xc). The drain material of a PMOS transistor is selected such that the drain material has an upper level Ed of the valence band that is higher than the upper level Ec of the valence band of the channel material of said PMOS transistor (Ed>Ec).

NMOS and PMOS transistors can be transistors of the normally on type or of the normally off type. In both cases (on and off), the drain material is chosen applying the rules set out above respectively to NMOS and PMOS transistors. For the source material, same material as the channel can be used. Advantageously, another material than that of the channel can be selected. In this case, transistors of the normally on type or of the normally off type have to be distinguished.

For normally on transistors, the source material of a NMOS transistor is preferentially selected such that the electronic affinity Xs(on) of the source material is higher than the electronic affinity Xc(on) of the channel material of said NMOS transistor (Xs(on)>Xc(on)). The upper level Es(on) of the valence

band of the source material of a normally on PMOS transistor is preferentially lower than the upper level Ec(on) of the valence band of the channel material of said PMOS transistor (Es(on)<Ec(on)).

For normally off transistors, the source material of a NMOS transistor is preferentially selected such that the electronic affinity Xs(off) of the source material is lower than the electronic affinity Xc(off) of the channel material of said NMOS transistor (Xs(off)<Xc(off)). The upper level Es(off) of the valence band of the source material of a normally off PMOS transistor is preferentially higher than the upper level Ec(off) of the valence band of the channel material of said PMOS transistor (Es(off)>Ec(off)).

These rules enable the drain and source materials to be selected such as to suit the channel material so as to give the transistor better performances. In particular, by choosing a suitable source material different from that of the channel, the velocity of the charge carriers in the channel is then automatically higher than the reference drift velocity which is the velocity obtained if the source material is of the same chemical nature as the channel material but strongly doped of opposite type. Moreover, the velocity of the charge carriers in the source is higher than the velocity of the carriers in the channel. The drain material is different from the channel material and the source material can be different from the channel material. The materials source and drain are also different from one another.

Table 1 indicates, in electronvolts, the electronic affinity X and the upper level E of the valence band of different materials able to be used to produce field effect transistors.

Material	Electronic affinity X	Upper level E of the valence band
Si	-4.05	-5.17
Ge	-4.13	-4.79
GaAs	-4.07	-5.49

Diamond-like C	0	-5.47
InSb	-4.59	-4.75

Table 1

For NMOS transistors, when the channel is for example made of silicon (electronic affinity X of -4.05eV), the drain can for example be made of germanium (X=-4.13eV), of gallium arsenide (X=-4.07eV) or of indium antimonide (X=-4.59eV). In all cases, the electronic affinity Xd of the drain material is thus lower than the electronic affinity Xc of the channel material (Xd<Xc). For a normally on NMOS transistor, the channel being made of silicon, the source can for example be made of diamond-like carbon (electronic affinity X of 0eV). Thus, the electronic affinity Xs(on) of the source material is higher than the electronic affinity Xc(on) of the channel material (Xs(on)>Xc(on)).

Table 2 indicates different preferential combinations of source and drain materials for a given channel material of a normally on NMOS transistor.

Channel material	N source material	N drain material
Si	Si, Diamond-like C	Ge, GaAs, InSb
Ge	Ge, Si, GaAs, Diamond-like C	InSb
GaAs	GaAs, Diamond-like C, Si	Ge, InSb
Diamond-like C	Diamond-like C	Si, Ge, GaAs, InSb
InSb	InSb, Si, Ge, GaAs, Diamond-like C	-

Table 2

For PMOS transistors, when the channel is for example made of silicon (upper level E of the valence band of –5.17eV), the drain can for example be made of germanium (E=-4.79eV) or of indium antimonide (E=-4.75eV). In all cases, the upper level Ed of the valence band of the drain material is thus higher than that (Ec) of the channel material (Ed>Ec). For a normally on PMOS transistor, the channel being made of silicon, the source can for

example be made of gallium arsenide (E=–5.49eV) or diamond-like carbon (E=–5.47eV), which corresponds to the condition Es(on)<Ec(on).

Table 3 indicates different preferential combinations of source and drain materials for a given channel material of a normally on PMOS transistor.

Channel material	P source material	P drain material
Si	Si,GaAs, Diamond-like C	Ge, InSb
Ge	Ge,Si, GaAs, Diamond-like C	InSb
GaAs	GaAs	Si, Ge, Diamond-like C, InSb
Diamond-like C	Diamond-like C, GaAs	Si, Ge, InSb
InSb	InSb, Si, Ge, GaAs, Diamond-like C	-

Table 3

In the case of normally off transistors, conditions for source material are the same as conditions for drain material, i.e. Xs(off)<Xc(off) (Xd<Xc) for a NMOS transistor and Es(off)>Ec(off) (Ed>Ec) for a PMOS transistor. Drain materials of normally off NMOS and PMOS transistors are, as indicated above, selected applying respectively the same rules as normally on transistors.

Thus, for a normally off NMOS transistor, when the channel is for example made of silicon, drain and source materials are selected for example among germanium, gallium arsenide and indium antimonide. For the source material, same material as the drain can be used. This choice enables to made transistor fabrication easier.

Table 4 indicates different preferential combinations of source and drain materials for a given channel material of a normally off NMOS transistor.

Channel material	N source material	N drain material
Si	Si, Ge, GaAs, InSb	Ge, GaAs, InSb
Ge	Ge, InSb	InSb
GaAs	GaAs, Ge, InSb	Ge, InSb
Diamond-like C	Diamond-like C, Si, Ge, GaAs, InSb	Si, Ge, GaAs, InSb
InSb	InSb	-

Table 4

For normally off PMOS transistors, when the channel is made of silicon, drain and source materials are selected for example among germanium, and indium antimonide. For the source material, preferentially same material as the drain is used.

Table 5 indicates different preferential combinations of source and drain materials for a given channel material of a normally off PMOS transistor.

Channel material	P source material	P drain material
Si	Si, Ge, InSb	Ge, InSb
Ge	Ge, InSb	InSb
GaAs	GaAs, Si, Ge, Diamond-like C, InSb	Si, Ge, Diamond-like C, InSb
Diamond-like C	Diamond-like C, Si, Ge, InSb	Si, Ge, InSb
InSb	InSb	-

Table 5

The invention is not limited to the combinations of materials indicated above, but applies whatever the materials liable to form a channel, a source or a

drain of a field effect transistor, provided that the two above-mentioned conditions are fulfilled. The source and drain materials can also be doped or not to further improve the performances of the transistor.

In a particular embodiment of a method for producing a transistor according to the invention, a first layer 1 designed to form the channel is deposited on a substrate 2, as represented in figure 1. The substrate can comprise an insulating thin layer on its surface, for example a layer of oxide having a high dielectric constant, for example alumina. Then a gate insulating layer 3 is deposited on the first layer 1. A conducting layer 4 is then deposited on the gate insulating layer 3. As represented in figure 1, the conducting layer 4 can be formed by superposition of a first conducting layer 4a and of a second layer 4b that can be conducting or not, which layer can be used as masking layer for etching. The conducting layer 4a can be deposited by low-pressure chemical vapor deposition or by epitaxy. An etching step enables the conducting layer 4 to be laterally delineated by means of a mask (not shown) so as to form the gate electrode 5. Then deposition of an insulating material on the flanks of the gate electrode 5 enables a lateral insulator 6 of the gate electrode 5 to be formed. The lateral electrical insulator 6 can be achieved by depositing a layer having a thickness corresponding to the thickness of the conducting layer 4 around the gate electrode 5, followed by etching by means of a mask (not shown)

In figure 2 etching of the gate insulating layer 3 in the zones of the substrate 2 not covered by the gate electrode 5 and the insulator 6 is represented. This etching can be performed using chlorinated mixtures and a hot cathode type technique.

Etching of the first layer 1, represented in figure 3, enables the channel 7 to be delineated laterally. The first layer 1 can be etched by anisotropic or isotropic etching, as represented in figure 3. By isotropic etching, a removal 8 of the first layer 1 is obtained underneath the gate insulating layer 3,

preferably creating a retraction extending up to underneath the gate electrode 5. Anisotropic etching can be performed by reactive ion etching.

Figure 4 represents deposition, for example by epitaxy on the substrate 2 on each side of the channel 7, of a source material 9a and a drain material 9b designed to respectively form the source and drain.

Anisotropic etching of the source material 9a and drain material 9b in the zones of the substrate 2 that are not covered by the gate electrode 5 and the lateral insulator 6 enables the source material 9a and drain material 9b to be delineated laterally and the source 10 and drain 11 to be formed, as represented in figure 5. Etching of the semi-conducting material in particular enables a transistor of small size to be obtained. Fabrication of the transistor is completed by formation of contact elements connected to the source 10 and drain 11, by deposition of a metal 12 on the substrate 2, planarization, for example by mechanical-chemical means, and etching of the metal 12.

When the source 10 and drain 11 of a transistor are formed by different materials, the method for producing the transistor preferably comprises deposition of a first mask on the substrate 2, at the place where the drain 11 is to be located, and deposition of the source material 9a on the substrate 2. The first mask can for example be a mineral mask made of silica (SiO_2), deposited by chemical vapor deposition. Deposition of the source material 9a can be performed by epitaxy. Then the first mask is removed, for example by means of a hydrofluoric acid solution (HF), and a second mask, for example made of silica, is deposited on the source material 9a. Then the drain material 9b is deposited, for example by epitaxy, and the second mask is removed. The materials 9a and 9b can then be etched anisotropically to respectively delineate the source 10 and drain 11, as previously. The transistor thus obtained can be coated with a thick layer of silica, in which the contacts are formed.

The invention applies more particularly to production of an integrated circuit preferably comprising PMOS type field effect transistors and NMOS type transistors according to the invention.

Claims

1. Field effect transistor comprising a source, a drain and a channel, respectively formed by source, drain and channel materials, transistor characterized in that the source, drain and channel materials being selected such that, for a NMOS type transistor, the electronic affinity (Xd) of the drain material is lower than the electronic affinity (Xc) of the channel material and such that, for a PMOS type transistor, the upper level (Ed) of the valence band of the drain material is higher than the upper level (Ec) of the valence band of the channel material.

2. Transistor according to claim 1, characterized in that source and channel materials of the transistor are the same.

3. Transistor according to claim 1, characterized in that transistor being of the normally on type, the electronic affinity (Xs) of the source material of a NMOS transistor is higher than the electronic affinity (Xc) of the channel material of said NMOS transistor and the upper level (Es) of the valence band of the source material of a PMOS transistor is lower than the upper level (Ec) of the valence band of the channel material of said PMOS transistor.

4. Transistor according to claim 1, characterized in that transistor being of the normally off type, the electronic affinity (Xs) of the source material of a NMOS transistor is lower than the electronic affinity (Xc) of the channel material of said NMOS transistor and the upper level (Es) of the valence band of the source material of a PMOS transistor is higher than the upper level (Ec) of the valence band of the channel material of said PMOS transistor.

5. Integrated circuit, characterized in that it comprises PMOS type and NMOS type field effect transistors according to anyone of claim 1 to 4.

Abstract

Field effect transistor with suitable source, drain and channel materials and integrated circuit comprising same

The PMOS or NMOS field effect transistor comprises a source (10), a drain (11) and a channel (7). The source, drain and channel materials are chosen such that, for a NMOS type transistor, the electronic affinity Xd of the drain material is lower than the electronic affinity Xc of the channel material (Xc<Xd) and such that, for a PMOS type transistor, the upper level Ed of the valence band of the drain material is higher than the upper level Ec of the valence band of the channel material (Ed>Ec).

(Figure 5)